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Optimizing Timing, Leakage Power and Area with Trade-Off Analysis in Energy and Area Efficient Chip Design

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***Abstract*— The underlying theme of the work is to obtain maximum performance with minimum leakage power consumption and no significant timing violations. This starts by loading an inefficient design having timing violations that exceeds 8000nS for setup and 45ns for hold in the post route stage, coupled with a staggering leakage power exceeding 200mW. Addressing these issues becomes the cornerstone of the initial phase, as several strategies are deployed to rectify the timing discrepancies, and optimize leakage power consumption, such that there exist no significant timing violations and the leakage power consumption stays below the 100mW mark.**

The next aim is to reduce the chip size, which shall take timing and leakage reduction db consecutively as input and perform a trade-off analysis between power and performance while reducing the chip area. The idea is to first optimize all three parameters individually and then analyze the compromises on the other two parameters, to obtain the best of all three worlds, where all three parameters can be optimized in a controlled fashion such that no parameter goes beyond a limit which might affect the design closure in later stages.

Index Terms*— db(Database), HVT(High Threshold Voltage), IC(Integrated Circuit), LVT(Low Threshold Voltage), mW(Milli Watts), nS(Nano Seconds), PnR(Place and Route), sdc(Synopsys Design Constraint), SVT(Standard Threshold Voltage), VLSI (Very Large-Scale Integration)

I. INTRODUCTION

In the world of VLSI design, the primary focus has always been on increasing speed to be able to deal with complex computing tasks efficiently. Semiconductor ICs that display various signal processing blocks and graphic units, provides us with powerful computing power. However, while it is true that these are good in terms of real-time processing, but they fall short when it comes to fast-working portable handheld devices that are power-hungry and where the idle battery drain is more. Portable electronics, such as smartphones and tablet computers, faces strict limitations on total power dissipation, which becomes a challenge for VLSI chip designers for maintaining optimal timing and performance while adhering to the leakage power consumption limits. As wireless portable devices continue to dominate the consumer electronics market, it becomes crucial to minimize the leakage power consumption of a device with reduced chip area, while being clean on the timing violations counterpart. This helps reduce the idle drain such devices.

As we try to reduce the chip size, leakage power increases with chances of getting timing violations with congestion hotspots and DRC violations. These violations need to be minimized as these issues might lead to a design closure failure in later stages. We aim for shrinking the core and die area while minimizing leakage power consumption, keeping timing and other parameters well under control.

II. LITERATURE SURVEY

In context of low power VLSI design, B. Padmavathi et al. [1] lists down the possible ways of power dissipation and the techniques that can be adapted for lowering power dissipation in a chip. The optimization techniques are characterized as system level, algorithm level. architecture level and technology level wherein every level uses different techniques to reduce the power [1]. Deepak Kumar et al. [2], focuses on the circuit design techniques that can be used to optimize power consumption of a chip. Since the standard cells have different drive strengths, sizes, delays, multiple-threshold volt- age and power consumption defined in their respective .lib file, designers characterize the gates to operate at voltages as much as 30% lower than the power-supply voltage [3]. Sumita Gupta and Sukanya Padave [4] in their work mentions about adiabatic circuits and the use of sleep transistors to reduce power dissipation. Coudert, Olivier [5] in his work mentions about timing and design closure in physical design flow. He also performed a survey of current flows, where he mentions about placement, logic optimization, buffering and clock tree synthesis.

III. WORK DONE

This work aims to lower the power consumption of the design without slowing down on its performance counterpart. After achieving a balance between timing and power, the next goal is to minimize the overall size of the design.

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However, as we keep reducing the size of the chip, there is a trade-off between timing and power, wherein the aim is to explore the best compromises and find the sweet spot where the design could be closed. Throughout these optimizations, the aim is also to ensure that the design follows all design rule constraints, avoiding any DRC violations or congestion hotspots. The final objective is to find an optimal configuration where all the parameters are in a balance state and design closure is not affected.

A. Initial Design with Violations

The initial project contains timing violations, both setup and hold and leakage power greater than 200mW. The design is loaded into the PnR tool to note down the initial values which serves as an initial reference point. All the violation values are for the post route stage.

Table I. Initial Run Violations

Violations	Comment/Value
Timing Violations	RRTNS: -8270.01nS HRRTNS: -47.51nS
Leakage Power	213.4mW
DRC Violations	187 Shorts
Congestion Hotspots	Nil

B. Optimizations

1) *Timing Violation Removal:* Investigating the design for timing violations, a timing report is generated by the PnR tool. Upon looking into the critical paths with maximum violations, it was seen that there are false paths and multicycle paths present in the design. The changes made to remove timing violations in the design are:
   - Defined missing exceptions from the sdc file in the design. This essentially means defining the false and multicycle paths present in the design but was not mentioned as exceptions in the sdc file. Those paths which has the starting path as a register clock pin and the ending path as SD or RD pins are defined as false paths as the ending pins are data check pins which are independent of clock. For asynchronous clocks with different time period, the setup analysis in done on the shortest window, while the hold analysis is done on the same clock edge. This shortest window checks sometimes lead to timing violations; hence the window needs to be relaxed by defining a multicycle path. These were defined explicitly in a script and sourced in the design. This helped clear most of the timing violations.
   - Performed timing aware placement, this essentially means setting more aggressive timing optimization parameters to the PnR tool while running the placement optimization flow. This clears out most of the timing violations, especially setup in the placement stage, which helped in later stages to meet the timing requirements.
   - Added place groups to bring standard cells with similar functionality and logic close to each other, this helped in removing long detours which effectively reduced the wirelength. This way setup violations are controlled in the initial placement stage.
   - For any long nets, buffers have been replaced by two inverters. This is done to reduce the overall stage delay as inverters have better driving capabilities which helped reduce the net transition time. This helped fix some setup violations.
   - Manually optimized the nets having sufficient setup margin, but failed the hold check by fewer picoseconds. This refers to inserting a buffer or delay cell before the sink pin followed by legalization. This way the hold violations are fixed.
   - Cell resizing is performed wherever it was necessary after checking the timing reports and the critical paths to get rid of timing violations in a particular path.
   - Allowed utilization of available higher metal layers for signal routing purpose.

   All the strategies are combined into the flow scripts and is allowed to run till detailed routing stage, after which the violation values are noted down.

Table II. Timing Optimization

Violations	Comment/Value
Timing Violations	RRTNS: +ve HRRTNS: 0nS
Leakage Power	193.4mW
DRC Violations	0 Shorts
Congestion Hotspots	Nil

2) *Leakage Power Reduction:* Leakage Power is reduced using an iterative process, where some low leakage power parameters are explicitly defined in a script and sourced in the design. This reduced the leakage to some extent, but not below 100mW, that has been considered as a target for this project. The changes made to reduce the leakage power are:
   - Defined more aggressive power optimization parameters in the PnR tool, which guided the tool to reduce power on maximum priority basis.
   - Performed cell swapping, wherein the LVT and SVT cells were swapped using HVT cells.
   - Restricted the use of high drive strength cells where it was not required.
   - Added place groups to pull standard cells close to each other, this reduce the wirelength which in turn helped in reducing leakage power. Also, this helped in removing some setup violations.
   - Swapped clock buffer cells having higher leakage power with ones having lesser leakage power.
   - Amongst all the HVT cells present in the design, those

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having more leakage is restricted for use in the design.

All the changes were made in the project building scripts and sourced till detailed routing. The results obtained in post route stage is:

Table III. Leakage Power Optimization

Violations	Comment/Value
Timing Violations	RRTNS: 0nS HRRTNS: 0nS
Leakage Power	98.5mW
DRC Violations	0 Shorts
Congestion Hotspots	Nil

3) *Core & Die Shrinking:* In this stage, the aim is to reduce the chip size. To do so, the timing optimized db is taken once and next the leakage power reduction db is taken. Steps followed for die shrinking are:

- Performed a flyline analysis to bring the macros having interconnections close to each other in the periphery of the core boundary.
- Added appropriate halo margins around the macros to ensure the pins get enough room for routing in later stages.
- Initiated floorplan with reduced boundary dimensions.
- Powerplanning the design.

The result obtained with the timing violation removal db is:

Table IV. Die Shrink - Timing Removal db

Violations	Comment/Value
Timing Violations	RRTNS: 0nS HRRTNS: 0nS
Leakage Power	183.11mW
Utilization	Core Utilization: 84.52%
DRC Violations	0 Shorts
Congestion Hotspots	Nil
MVT Cells (%)	LVT: 7.25% SVT: 5.65% HVT: 86.21%

The result obtained with the leakage power reduction db is:

Table V. Die Shrink - Leakage Power Reduction db

Violations	Comment/Value
Timing Violations	RRTNS: 0nS HRRTNS: -0.308nS
Leakage Power	111.09mW
Utilization	Core Utilization: 60.43%
DRC Violations	0 Shorts
Congestion Hotspots	Nil
MVT Cells (%)	LVT: 1.23% SVT: 7.75% HVT: 85.69%

The results obtained after shrinking the die doesn't contain any DRC violations or congestion hotspots. However, once the die is shrunk more, DRC violations comes into the picture in terms of shorts and minimum space violations. This way we achieve a point where no further shrinking could be performed.

C. Trade-Off Analysis

In VLSI Physical Design, we settle for a parameter that tops the priority list. Once the chip size is reduced to maximum possible extent wherein no further reduction is possible with- out causing DRC violations, is a point where we can analyze for the tradeoffs. In this work few techniques were used to control fluctuations of the other parameters. This can be confirmed by the results obtained while using different dbs in the project. Keeping a design clean from any timing violations

is a must for design closure, hence we should use the timing clean db instead of leakage power reduction db, as it helped to gain more core utilization percentage without violating the timing counterpart.

IV. CONCLUSION

In conclusion, this work has successfully achieved a significant reduction in leakage power, by bringing it below 100mW while adhering to timing constraints. Also, the size of the chip has been reduced significantly such that the core utilization remains above 80%. This accomplishment sets the stage for further advancements and optimizations in the chip design process. It can be seen from the obtained result that:

- As we try to optimize timing, leakage power consumption is increased if we allow cell swapping and start using the LVT cells to fix timing violations. To keep the leakage power under control, we can go for the other optimization techniques instead of swapping SVT and HVT cells with the LVT cells. Only if there are some critical paths responsible for high-speed operations, LVT could be considered as a choice.
- As we try and reduce the leakage power consumption, we can go for cell swapping. This significantly helps in reducing the leakage power. This however can cause some timing violations to come into picture, which can be taken care off at later stages by inserting delay cells or buffers.
- As we reduce the chip size, we should use the timing clean db instead of leakage power reduction db. This way we can reduce the chip size more without creating any other violations.
- Flyline analysis and keeping a halo margin is a must while performing die shrink as it helps avoid any un- wanted DRC in routing stage.

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